Adaptive & Analytical Design of Phase Locked Loop with Higher Frequency for Generating Many Outputs using Performative VCO for Wireless Applications

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Abstract— This paper presents an adaptive design of analytical phase locked loop with more outputs with highly frequencies in the concept of low power and increased speed. Considering power consumption is a crucial aspect of high-frequency network design, especially in the context of microprocessor advancements, both static and dynamic power dissipation can be directly affected by reducing power consumption, leading to an increase in the circuit's overall efficiency. So, Design and Analysis of a low power phased-locked loop with multiple output(s) is basically implemented by modifying closed loop frequency control system PLL-blocks to improve these parameters with 45nm technology.

***Index Terms*— Single Integrated Circuit (SIC), Complementary Metal–Oxide–Semiconductor (CMOS), Digital-Phase Locked Loop (D-PLL), Charge Pump (CP)**

I. INTRODUCTION

The ability of phase loops (PLLs) to precisely control the phase and frequency relationship between independent signal sources makes them extremely useful in many applications, including communication and instrumentation. Applications like frequency synthesis and phase recovery rely on PLLs in the microwave range. Although advancements in Digital Signal Processing (DSP) have been noticeable, the technology still cannot process and generate the necessary Radio Frequency (RF) signals for wireless data transmission. The optimization and implementation of PLLs for various applications, such as clock distribution in microprocessors and microwave frequency synthesis, demonstrate their crucial role in contemporary communication and electronic systems. As RF engineering and digital communications continue to evolve, PLLs are becoming more and more important tools due to the continuous improvements in their performance.

II. PHASE LOCKED LOOP METHODOLOGY

A Phase-Locked Loop (PLL) is a control system that generates an output signal whose phase is fixed relative to the phase of an input signal. It generates the zero (or) constant Phase difference between Reference & Output Signals. By using a frequency divider, a PLL can generate a stable frequency that is a multiple of the input frequency. Thus, the research describes the basic component of the PLL and how to build and analyze the proposed PLL using 45 nm VLSI technology. In particular, delves into the basic components of a PLL, offering insights on how to construct and evaluate a proposed PLL design utilizing 45 nm VLSI technology. By exploring the intricacies of PLL construction and analysis, this study aims to enhance the understanding and application of PLLs in advanced technological contexts.

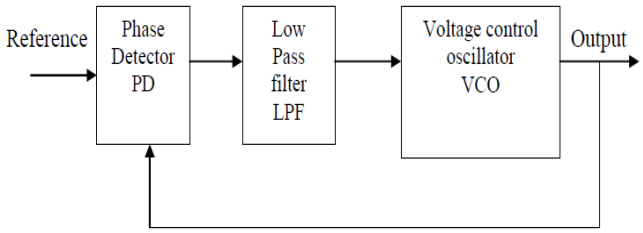

Fig 1: Basic PLL

The intricate world of Very Large-Scale Integration (VLSI) is a multi-layered tapestry, woven from logic gates, transistor circuits, and physical layouts. For our Phase-Locked Loop (PLL), we wield the Microwind 3.1 VLSI Backend software as our digital sculpting tool. This software empowers us to translate abstract design concepts into tangible silicon blueprints, operating at the minuscule scale of 45 nanometers.

Sr. No.	Parameter	Value
1	VDD (V)	**0.85-1.2 V.**
2	Ioff N (nA/um)	**5-100**
3	Ioff P (nA/um)	**5-100**
4	Gate dielectric	**SiON, HfO_2**
5	No. of metal layers	**6-10**

Table 1: 45 nm Technology's Most Important Characteristics

A multitude of paths converge on the creation of a phase-locked loop. The chosen tool, MICROWIND 3.1, is a digital sculptor's system, allowing to mold integrated circuits with precision at the physical level. Within its virtual realm, a

rich library of logic and analog components awaits, ready to be combined and simulated.

These architectural guidelines are known as design rules. They dictate the minimum size of wires, the spacing between components, and other critical parameters. Violate these rules, and the city faces collapse – in this case, circuit failure.

Design rules are typically expressed in two languages: microns, the familiar units of length, and lambda, a scalable measure. While lambda once promised universal adaptability, the complexities of modern chips have made it less reliable.

MOS Model 1 Parameter			
Parameter	**Definition**	**Typical Value 0.12 NMOS**	**PMOS**
VTO	Threshold Voltage	0.4V	0.4V
U0	Carrier mobility	0.06m^2 V/s	0.06m^2 V/s
TOX	Gate oxide thickness	2nm	2nm
PHI	Surface potential at strong inversion	0.3V	0.3V
GAMMA	Bulk threshold parameter	0.4 $V^{0.5}$	0.4 $V^{0.5}$
W	MOS channel width	1 µm	1 µm
L	MOS channel length	0.12 µm	0.12 µm

Table 2: MOS Level 1 Parameters in MICROWIND3.1

III. DEVELOPMENT OF PHASE DETECTOR AND FILTER

In designed Phase-Locked Loop (PLL), an XOR gate is employed. This gate produces a stable square-wave signal, labeled VPD, when there is a phase shift of one-quarter period (90 degrees or π/2) between the clock input circuit and the signal input divIn. However, deviations from this specific phase shift result in an erratic output.

As depicted in Figure 2, initially, the average output of the XOR gate, VPD, hovers around zero. As the phase difference between ClkDiv and ClkIn nears π/2, the output PD V rises to VDD/2 and then continues to increase up to VDD.

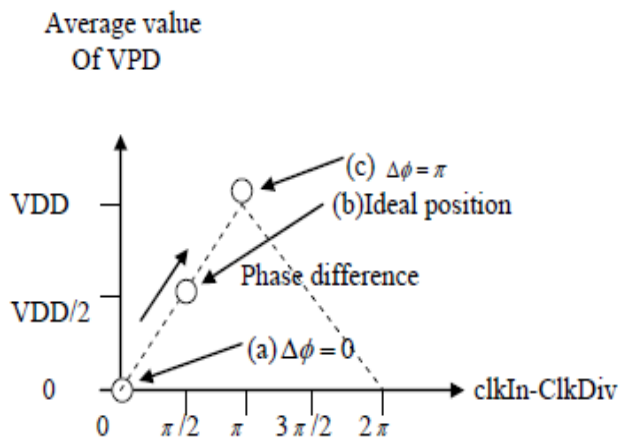

Fig 2: Performance of the XOR Phase Detector

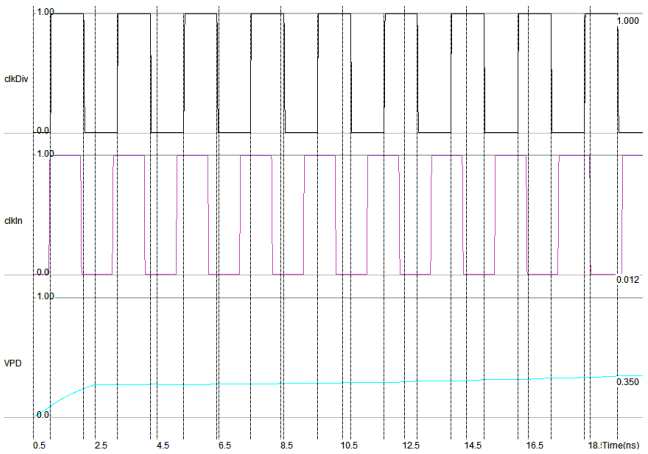

Fig 3: Voltage verses Time Response of Phase Detector

IV. DEVELOPMENT OF A LOW-POWER PHASE-LOCKED LOOP WITH FOUR OUTPUTS

To navigate this challenge, engineers have developed ingenious strategies. Figure 4 showcases one such innovation: a meticulously optimized Phase-Locked Loop (PLL) circuit built on a 45nm fabrication process. This energy-efficient design, capable of driving four simultaneous outputs, is a testament to careful circuit layout and transistor selection. Adhering to strict design guidelines and employing a precise blend of 29 NMOS and 28 PMOS transistors, this PLL represents a balanced approach to performance and power consumption in the era of shrinking silicon.

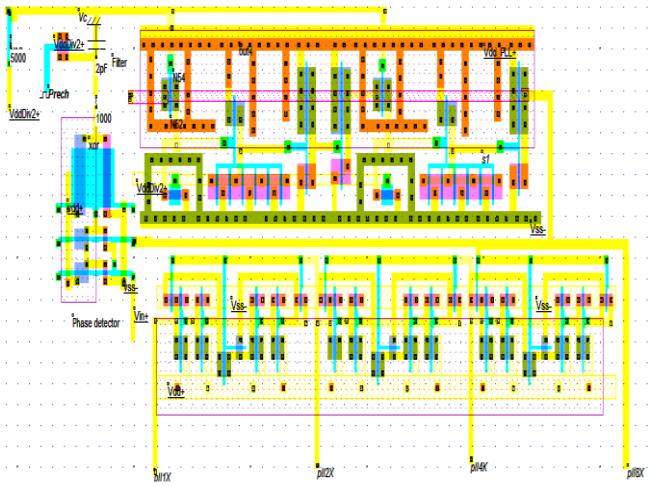

Fig 4: The Optimum, High Efficient Layout Design of Low Power PLL with Four Outputs using 45nm VLSI Technology

Fig 4 shows the optimum, high efficient chip design of low power PLL with four multiple output using 45nm VLSI technology. This layout design is implemented using 29 NMOS along with 28 PMOS BSIM4 transistors with optimum dimensions of transistors and metal connections according to the lambda-based rules of microwind 3.1 software. This versatile PLL can generate a multitude of frequencies, from the base 1x to higher octaves like 2x, 4x, and 8x, as well as the complementary 1x90 tone. These harmonious frequencies are essential for the intricate dance of multiphase clocking circuits. For instance, a simple D-flip flop can divide the rhythm in half, creating a new beat from the original pulse.

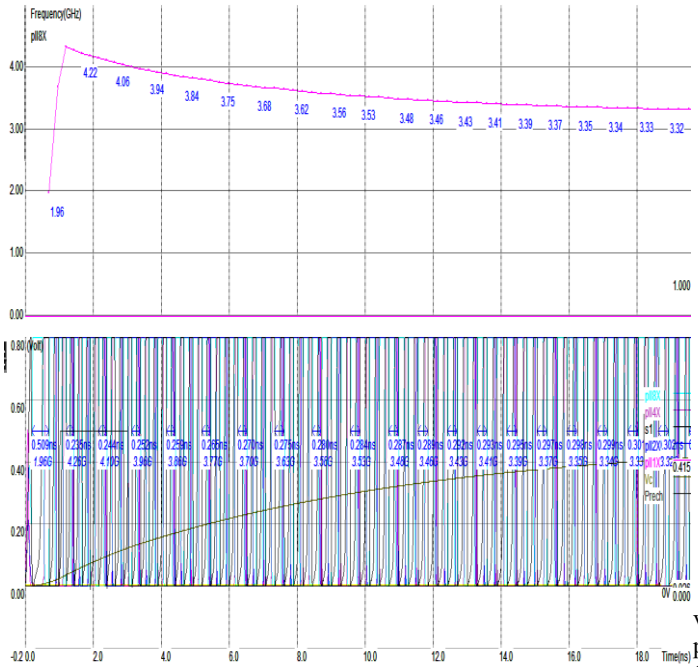

Fig 5: Frequency Dynamics of PLL8x Node in a Quad-Output PLL

V. RESULT

A prevalent method for minimizing power consumption is by decreasing the supply voltage. However, in CMOS circuits, this reduction in supply voltage typically results in diminished performance. Supply voltage fluctuations affect the Voltage-Controlled Oscillator's frequency.

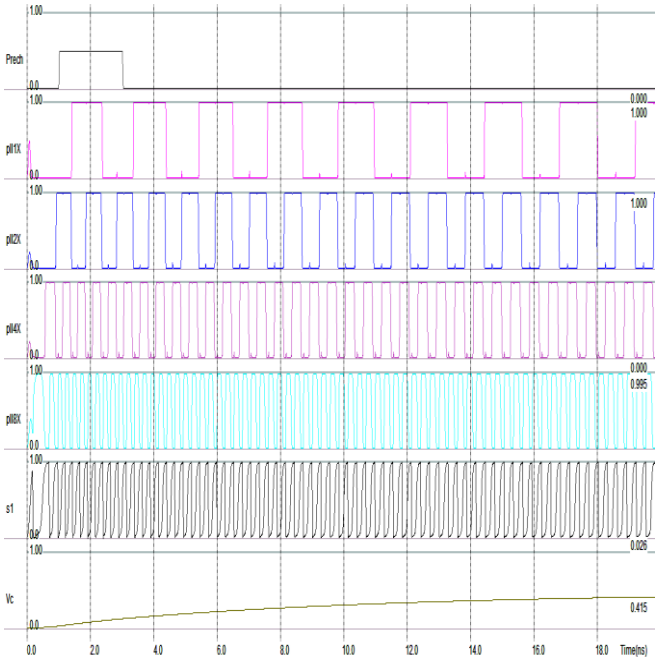

Fig 6: Voltage verses Time Response for PLL with Multiple Output

If detail verification of parameters would not completed then again fallow the first step with different methodology. As a result of technology scaling, there are increased process variations of circuit parameters such as the transistor channel length and transistor threshold voltage. The increased process variations can have a significant effect on circuit performance and power variations also have an impact on how exactly a parallel system should be designed.

S. No	Existing PLL System		Proposed PLL System	
	VDD (Volts)	Freq (GHz)	VDD (Volts)	Freq (GHz)
1	1.5	2.510	0.8	3.306
2	1.7	2.510	0.9	3.306
3	1.9	2.510	1.0	3.306
4	1.10	2.510	1.1	3.306
5	1.12	2.510	1.2	3.306

Table 3: Comparison of Existing & Proposed PLL Systems with VDD Supply Voltages & Frequencies

For designing CMOS VLSI systems that operate with low supply voltages, chip implementation is directly constrained by the processing technology and device characteristics. The behavior of CMOS devices is modeled through various equations addressing factors such as threshold voltage, short-channel effects, narrow-channel effects, electron temperature effects, hot carrier effects, and capacitance models. Specifically, the BSIM SPICE models, particularly BSIM4, are employed for deep-submicron CMOS transistors.

For achieving low power consumption, BSIM4 transistors are preferred, despite a slight compromise in frequency. Additionally, the proposed circuit includes a shutdown input that enables the PLL to hold its state. the effects of changes in VDD on the frequencies of the PLL circuits designated as PLL8x, PLL4x, PLL2x, and PLL1x, respectively. These figures confirm the PLL's robust stability across different voltage levels. Additionally, a parametric analysis of the PLL's performance reveals that with a VDD of 1V, the power dissipation is measured at 0.211 milliwatts. This low power dissipation further indicates that the PLL circuits are designed for efficient power consumption.

VI. CONCLUSION & FUTURE SCOPE

In these days, there are many digital products, which are implemented by CMOS VLSI technology, in the market. Currently, CMOS VLSI is progressing at fast rate for decades and dominating most of markets in digital circuit areas. In a constant voltage scaling, the vertical and later electric fields are increased, which reduced to oxide reliability. Low power supply voltage is required necessarily. For the design of CMOS VLSI systems using low power supply voltage, the implementation of chips is directly limited by processing technology and devices. The modeling of CMOS device behaviors are analyzed with the equations including threshold voltage, short channel effect narrow channel effect, electron temperature effect, hot carrier effect and capacitance model. Finally, the BSIM SPICE models BSIM4 are summarized for deep-submicron CMOS transistor. For low power, lowleakage transistors BSIM4 are used and compromised on little bit frequency. Also there is shutdown input in proposed circuit which brings the PLL to hold.

In future PLL designing size can be reduced to further nm technology with increase in performance, reduction in size, high stability for different medical, electronic and electrical applications. Phase Locked Loop can be extended to Digital systems with the modelling of CMOS device behaviours, equations including threshold voltage, short channel effect narrow channel effect, electron temperature effect, hot carrier effect and capacitance model in better manner.

VII. REFERENCES

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